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ANALYSIS OF POWER AND DELAY IN A RECONFIGURABLE SRAM ARRAY ARCHITECTURE

Anarga.S[1] , V.J Arul Karthick[2]

PG-Scholar, Electronics and communication, SNS College of technology, Coimbatore, India[1]

Assistant professor, Electronics and communication, SNS College of technology, Coimbatore, India[2]

Abstract: SRAM arrays generally occupy a large portion of the Socs and are also a significant source of power dissipation. The most commonly used arrays constitute the 6T SRAM cells. In order to achieve high reliability and long battery life for portable applications, the design of low power SRAM arrays are required. Thus reconfigurable SRAM arrays are constructed here and a comparison is made for the delay, power with that of the other arrays. This reconfigurable SRAM array is used as a memory element in applications such as ALU Design.

Keywords: Digital forensics, image compression, SPIHT compression, DWT coefficients.

I. INTRODUCTION

Many electronic gadgets usually rely on stored information which is mainly data. The digital information is stored in memory devices. Static Random Access Memory (SRAM) is used mainly as high-speed memory. SRAM is preferred over DRAM for the following reasons:(i) It doesn't require to be refreshed in order to hold the data which is responsible for its enhanced read/write speed (ii) Also consumes less power[1]. Basically the disadvantages of conventional arrays using 6T SRAM cells in which there is a "false read" before a write operation due to a bit line and word line timing mismatch. During the write operation in 6T SRAM, the instant at which the word line precedes ahead the column-select in timing, the cell starts reading the data .At that time when the bit line drops, "false read" occurs before the write operation. This particular drawback of 6T is overcome by the 8T-CDC cell; the early word line (GWLE) will be gated by the column select and thus "false read" before write does not happen here. Generally Column select/half-select is commonly used in SRAMs to provide SER protection and also to enable area efficient utilization. The advantages of the 8T-CDC cell compared to that of 6T cell are: (a) allows the designer to integrate it in a column select fashion and (b) offers/maintains SER protection ;while the other advantages include1) maximizes array efficiency, 2) eliminates the read disturb to the unselected cells, and 3) reduces power with simplification in peripheral logic [2]. The 8T CDC with bit line decoupled current sensing amplifier is seen to more advantageous when compared to 8T CDC in terms of power as well as delay. Thus we go for the reconfigurable SRAM array architecture using 8T CDC with bit line decoupled current sensing amplifier cell. A small number of redundant columns of SRAM cells are to replace a column of cells that contains a cell with manufacturing faults (Eg: stuck-at-faults). The reconfigurable SRAM array is then reconfigured to access a redundant column instead of the column containing the defective cell. The arithmetic logic unit (ALU) is the core of a CPU in a computer. A 4-bit ALU has been designed so the memory array coupled to it should also be capable of storing 4 –bits henceforth a 4x1 reconfigurable array has also been designed..

II. RECONFIGURABLE SRAM ARRAY

The basic element of the array is its 8T CDC with current sensing amplifier cell. The power of the above array is compared with that of the array with 6T, 6T CDC,8T CDC cells. So basically the 6T SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. The storage cell has two stable states which are usually denoted as 0 and 1.The two additional access transistors control the access to a storage cell during read and write operations. This cell offers better electrical performances (speed, noise immunity, standby current) than a 4T SRAM structure. Column Select(Half-selected) cells are

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the cells on the activated word-line whose bit lines are not activated. To solve the problems caused by the half selected cells we go for the decoupling logic thus giving rise to column decoupled cell(CDC)[3].Actually in the 6TCDC the read disturb is decreased to an extent and it decreases due to the discharge in the bit line capacitance which is caused by the read current[1]. Whereas in the 8T CDC cells the local word-line for only the selected cells is activated, thus effectively protecting the half-selected SRAM cells from the read disturb problem that exists in 6T cell due to word-line sharing. It is also possible to swap the input and supply pairs of the gated inverter which in turn reduces cost and extra delay stage and power. Figure 1 shows a 8T CDC with bit line decoupled current sensing amplifier cell, the current sense amplifier is used as it is more advantageous compared to the voltage like there is reduction in bit-line voltage swing and also major reduction in the sensing delay. These benefits in turn give rise to lower dynamic power consumption and increased speed. The reason of using a tail NMOS device in the cell is that it gives a smaller area comparing to a PMOS device The bit-line differential signal is been induced at nodes of the latch, thereby turning off one of the NMOS transistor and turning on the other in the latch. Concurrently, both the PMOS transistors attached to the nodes of the latch are turned off thus decoupling the bit-lines from the high-swing output nodes.

The above mentioned PMOS transistors helps in reducing the impact of the bit-line capacitances on the switching activity, thereby significantly reducing both sensing delay and power consumption. Each memory cell shares electrical connections with all the other cells in its row and columns. The horizontal lines connected to all the cells in a row are called the word lines, and the vertical lines along which the data flow in and out of the cells are called bit lines. Each cell can be uniquely addressed, as required, through the selection of an appropriate word and a bit line[6]. The memory array nominally uses a square or a rectangular organization to minimize the overall chip area and for ease in implementation.

Thus the 4x1 reconfigurable SRAM arrays or may it be the conventional SRAM arrays all are having a rectangular organization. Most RAMs operate such that the row address enables all cells along the selected row. The column address is used to select the particular column containing the desired data bit. Additional circuitry, including sense amplifiers, control logic, and tri-state input/output buffers, are normally placed along the sides of a cell array.

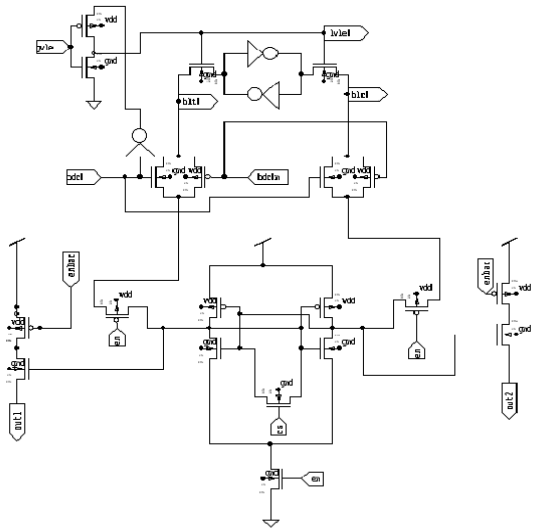

Fig.1 8T CDC with bit line decoupled current sensing amplifier

A. SRAM Fault Removal Using Redundancy

There have been various redundancy techniques adopted in DRAM and SRAM to repair defective cells caused by stuck-at-faults[4]. However, the VDD_{MIN} reduction resulting from the use of such alternate SRAM designs comes at the cost of significant increases in SRAM cell area. One standard technique we leverage is the use of redundant columns of SRAM cells. A failure in any of the cells in a column of the memory will make that column faulty. In a memory, the redundant columns are used to improve the fault tolerance of the memory[9] .An example of a column redundancy implementation in an SRAM array using a "shift redundancy "scheme is shown in figure 2 [5].Generally, if any cell in a column fails, the adjacent column replaces the failed column. In turn, the next column is replaced with the column one next to it, and so on. This goes on until a redundant column replaces the last non-redundant column in a segment as depicted in the figure 2.

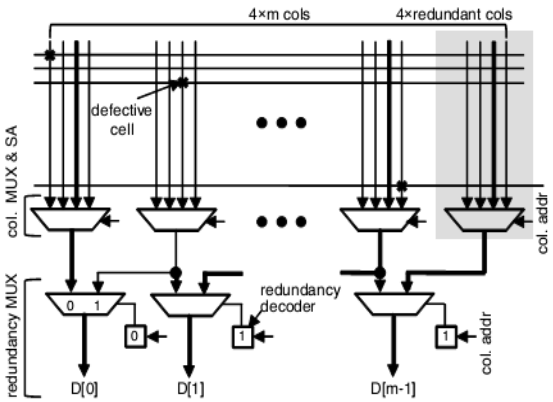

Fig.2 Example of Column Redundancy Implementation in SRAM Array

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The redundancy MUX in the example is generally programmed by one-time-programmable(OTP) fuses and the redundancy decoder comprises of 4-bit scan flip-flops. A memory having multiplexed address inputs uses a column decoder which is deactivated during row address time and becomes activated during column address time The column address is being given as a select input to the MUX which in turn is obtained from a column decoder. Along with the column address, it steers each bit from every column, including the redundant one, to the correct corresponding bit location of the I/O bus. The bold lines shown in the Figure 2 indicates the data flow after the third column in the second bit is fixed by a redundant column. Also only one redundant column could be used per m columns due to the increasing complexity of the steering logic[10].

B. Alu Design

A 4-bit ALU as shown in figure 3 has four stages, each stage consisting of the following parts: a) input multiplexers b) full adder and c) output multiplexers. The ALU here performs four arithmetic operations: ADD ,SUBTRACT, INCREMENT and DECREMENT and also four logical operations performed are EXOR, EXNOR, AND and OR[7]. The input and output sections of the ALU consist of 4 to 1 and 2 to 1 multiplexers. Taking area efficiency into account ripple carry adder is preferred here. The inputs of the 4 to 1 multiplexer, Logic '1' and Logic '0' are used for the INCREMENT and DECREMENT operations respectively. The complement of B is used for SUBTRACTION operation. The full adder[8] here performs the SUBTRACT operation by two's complement method. The INCREMENT operation is done by adding a '1' to the addend and DECREMENT is viewed here as a subtraction operation.

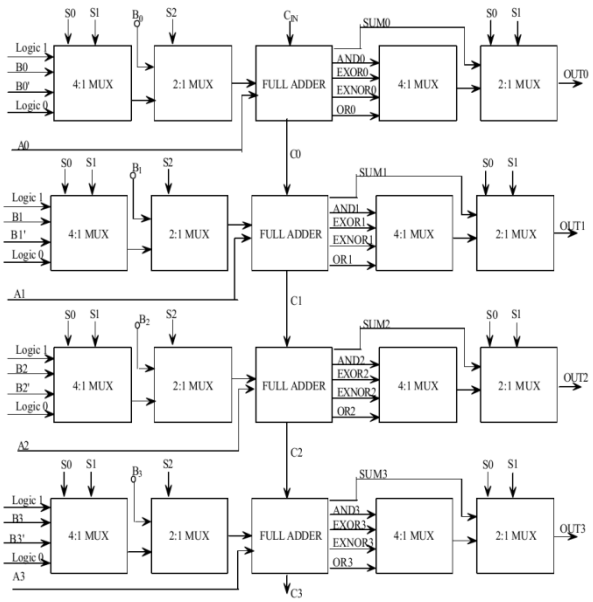

Fig.3 Block Diagram of the 4-bit ALU Design

The outputs of the full adder are SUM, EXOR, EXNOR, AND and OR. Based on the condition of the select signals, the multiplexer selects the respective inputs and gives it to the full adder which then passed on to the output stage multiplexers which selects the appropriate output .Generally only 1 bit memory elements are coupled to the ALU Design like the d flip flop or a latch as shown in Figure 4. As a 4 bit ALU is been designed here a memory element of 4 bit capacity is required. For which the reconfigurable SRAM array with less power consumption and delay is been coupled to the ALU. The input to the ALU is basically fed from the memory element and thereafter the output from the ALU again gets stored in the memory element and to stop the continuation in the cycle, the word line of the memory element is disabled as the word line needs to be enabled for either read or write operation to take place.

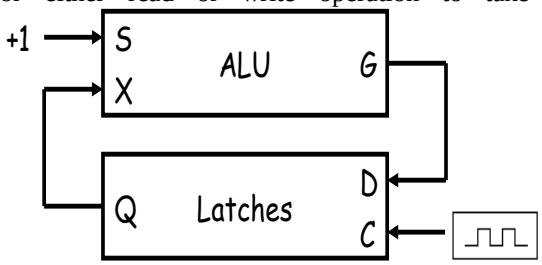

Fig.4 ALU with Latch as memory element

III. RESULTS AND DISCUSSIONS

In order to measure the power during a write cycle in this cell, two different voltage sources are created: one for the hardware external to the memory cell (such as the input logic) and one for the memory cell itself. This in turn allows the power to be monitored for the memory cell alone .The power measured is the total power used during one write cycle. The delay is the time it takes to write to a cell.

TABLE I: COMPARISON OF POWER AND DELAY IN VARIOUS ARRAYS

Arrays	Average Power(W)	Delay(sec)	Product
4x1 SRAM array with 6T cells	8.53*10^3	1.36	11.6*10^3
4x1 SRAM array with 6T CDC cells	9.47*10^3	0.79	7.48*10^3
4x1 SRAM array with 8T CDC cells	2.54*10^5	1.02	259.08*10^3
4x1 Reconfigurable SRAM Array with 8T CDC with Bit Line Decoupled Current Sensing Amplifier cells	6.709*10^1	0.85	5.702*10^1

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Thus from the above table it is seen that the power is considerably reduced in the reconfigurable SRAM array and also the delay is less compared to that of the 4x1 array having 8T CDC cell. Certainly when the power and delay product is compared the reconfigurable SRAM array seems to be the best among the others.

The input and output waveform of a 4x1 reconfigurable SRAM array having 8T CDC with bit line decoupled current sensing amplifier cell as shown in figure 5 in which both the performance of the 8T CDC cells as well as the current sense amplifier are showcased here.

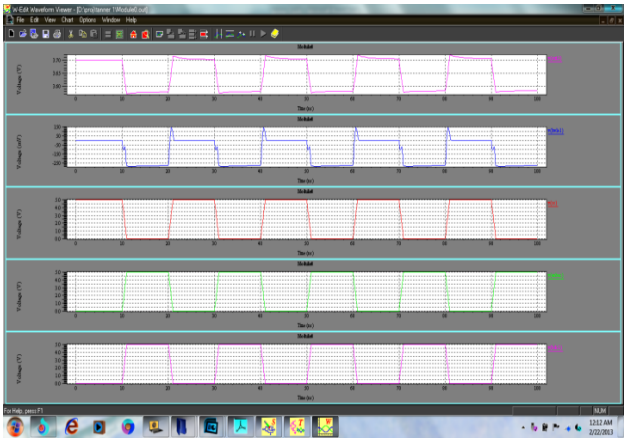

Fig. 5 Input and Output Waveform of Reconfigurable SRAM Array

The input and output waveform of the reconfigurable SRAM array with the redundant columns introduced in it thus making the array fault tolerant. Thus the waveform as shown in figure 6 is evident of both faulty and fault free inputs and also by the implementing the shift redundancy technique the fault is been removed and gated out as the output.

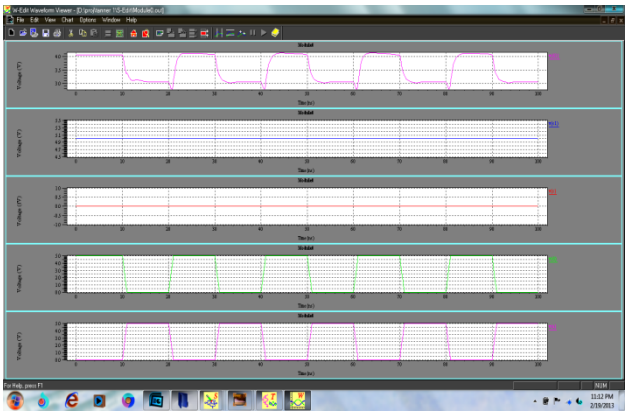

Fig. 6 Input and Output Waveform of Reconfigurable SRAM Array with Redundant Columns

The input and output waveform of the addition operation is been showcased in the figure below and as it is one of the prominent operations of the ALU it is been shown here .This takes place in the full adder module of the ALU unit.

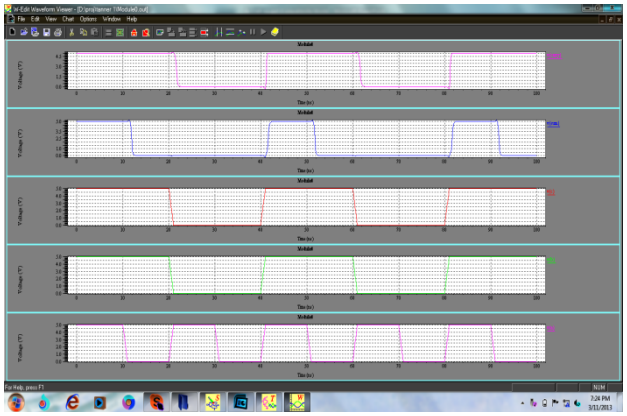

Fig.7 Input and Output Waveform of The ALU unit

A. Simulation Software

Tanner T-Spice has key features such as device state plotting,real-time waveform viewing and analysis, and command tools for simpler SPICE syntax creation, T-Spice save time and money during the simulation phase of your design flow. The role of T-Spice is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit .T-Spice accepts standard SPICE, table based, and user-defined models. The results of device model evaluations are stored in tables and reused. Because evaluation of device models can be computationally expensive, this technique can yield dramatic simulation speed increases. The memory used by T-Spice tables is optimized by storing only those points which are actually needed. T-Spice allows you to specify which devices use tables. The simulation system includes S-Edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform probing.

IV . CONCLUSION

Thus in this paper the reconfigurable SRAM array is seen to be consuming less power and delay which is an important factor for the low power circuits as well as in the field of the VLSI. Therefore this SRAM array is employed in an application such as ALU Design. One drawback is that the number of transistors get increased in case of the application which could be replaced using MIFG CMOS transistors which cannot be constructed in Tanner T-Spice which could be done using P-Spice software and which leads to lesser number of transistors leading to an enhanced area compared to this.

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BIOGRAPHY

Anarga. S, pursuing final year Master of engineering in VLSI Design, SNS College of Technology, Coimbatore.

V. J. Arul Karthick, Working as Assistant Professor in SNS College of Technology, Coimbatore.